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10/550,178	09/21/2006	Mark Alan LaMonte Johnson	297/172PCT/US	8335

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2894	

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03/16/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/550,178	JOHNSON ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2894	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/21/05;2/6/06;2/27/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

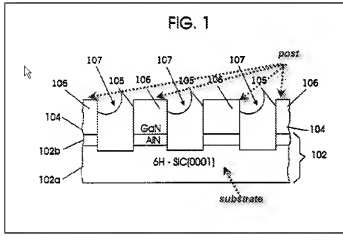
DETAILED ACTION

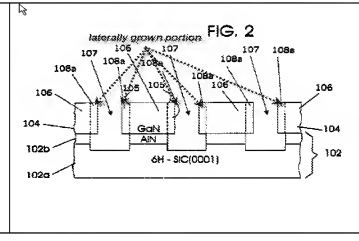
Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 9-12, 15, 30-33, 36, 40, 41, 50, 53 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Zheleva et al. (US 6,265,289).





Re claim 9, Zheleva et al. disclose a semiconductor structure comprising: a substrate (102 104) having dislocation defects spaced apart by an average distance (i.e., the substrate 102 104 region of the GaN layer has dislocation and the etched part of dislocation is spaced apart) characteristic for the substrate; at least one post (106) included on the substrate, the post having a width less than the average distance separating the dislocation defects (i.e., the width of 106 is less than the width of opening) characteristic for the substrate (see Figs. 1 and 2); and (c) a

laterally grown portion (108a) extending laterally from the post and over the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Re claims 10 and 11, as applied to claim 9 above, Zheleva et al. disclose all the claimed limitations including wherein the post is formed by lithography.

With respect to the post formed by sub-micron lithography or edge definition lithography the process claim has no patentable weight for the product. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Re claim 12, as applied to claim 9 above, Zheleva et al. disclose all the claimed limitations including wherein the laterally grown portion is spaced vertically from the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Re claim 15, as applied to claim 9 above, Zheleva et al. disclose all the claimed limitations including wherein the laterally grown portion comprises outermost flat fronts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Re claim 30, Zheleva et al. disclose a semiconductor structure comprising: a substrate (102) having a dislocation defects spaced apart by an average distance characteristic for the substrate; a plurality of posts (106) included on the substrate (102); and a laterally grown portion (108a) extending laterally from each post and over the substrate, wherein a spacing between adjacent laterally growth portions from adjacent posts is less than the average distance

separating the dislocation defects characteristic for the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Re claims 31 and 32, as applied to claim 30 above, Zheleva et al. disclose all the claimed limitations including wherein the post is formed by lithography.

With respect to the post formed by sub-micron lithography or edge definition lithography the process claim has no patentable weight for the product. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Re claim 33, as applied to claim 30 above, Zheleva et al. disclose all the claimed limitations including wherein the laterally grown portion is spaced vertically from the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Re claim 36, as applied to claim 30 above, Zheleva et al. disclose all the claimed limitations including wherein the laterally grown portion comprises outermost flat fronts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Re claim 40, as applied to claim 31 above, Zheleva et al. disclose all the claimed limitations. With respect to the post formed by sub-micron lithography or edge definition lithography the process claim has no patentable weight for the product. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of

production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Re claim 41, as applied to claim 30 above, Zheleva et al. disclose all the claimed limitations including wherein the coalesced layer has reduced dislocation defects (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Re claim 50, Zheleva et al. disclose a method for forming a laterally grown semiconductor structure comprising: providing a substrate (102) having dislocation defects spaced apart by an average distance characteristic for the substrate (102); forming at least one post (106) on the substrate (102), the post having a width less than the average distance separating the dislocation defects characteristic for the substrate (102); and growing a laterally grown portion (108a) from the post extending laterally from the post and over the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Re claim 53, as applied to claim 50 above, Zheleva et al. disclose all the claimed limitations including growing the laterally grown portion to be spaced vertically from the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Re claim 56, as applied to claim 50 above, Zheleva et al. disclose all the claimed limitations including comprising growing the laterally grown portion structure wherein the laterally grown portion comprises outermost flat fronts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 13, 14, 16, 34, 35, 37, 51, 52, 54, 55 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zheleva et al. (US 6,265,289)

Re claim 13, as applied to claim 9 above, Zheleva et al. disclose all the claimed limitation. Furthermore, the claimed post width dimension can be routinely optimized in order to achieve predetermined size of the post.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious

absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claims 14 and 16, as applied to claim 9 above, Zheleva et al.disclose all the claimed limitations including growing the laterally grown portion.

With regard wherein the laterally grown portion comprises outermost pointed fronts or generally triangular shape Examiner takes an Official notice because it is well-known in the art that group III-V semiconductor such GaN other are can be easily grown hexagonal or pyramidal structure having pointed face See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 34, as applied to claim 30 above, Zheleva et al. disclose all the claimed limitations including growing the laterally grown portion.

Furthermore, the claimed post width dimension can be routinely optimized in order to achieve predetermined size of the post.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an

unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claims 35 and 37, as applied to claim 30 above, Zheleva et al. disclose all the claimed limitations including growing the laterally grown portion.

With regard wherein the laterally grown portion comprises outermost pointed fronts or generally triangular shape Examiner takes an Official notice because it is well-known in the art that group III-V semiconductor such GaN other are can be easily grown hexagonal or pyramidal structure having pointed face See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claims 51 and 52, as applied to claim above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

With regard growing the post by sub-micron lithography or edge definition lithography. Examiner takes an Official notice because it is well-known in the art that the sub-micron lithography or edge definition provides structure or pattern within the nano regime . See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 54, as applied to claim 50 above, Zheleva et al. disclose all the claimed limitation. Furthermore, the claimed post width dimension can be routinely optimized in order to achieve predetermined size of the post.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claims 55 and 57, as applied to claim 50 above, Zheleva et al.disclose all the claimed limitations including growing the laterally grown portion.

With regard wherein the laterally grown portion comprises outermost pointed fronts or generally triangular shape Examiner takes an Official notice because it is well-known in the art that group III-V semiconductor such GaN other are can be easily grown hexagonal or pyramidal structure having pointed face See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

5. Claims 1-8, 17-29, 38, 39, 42-49 and 58-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zheleva et al. (US 6,265,289) in view of Brueck et al. (US 5,705,321).

Re claims 1, 5, Zheleva et al. disclose a semiconductor structure comprising: a substrate (102) including at least one post (106) (see Fig. 1), the post size and spacing having predetermined dimension of size and width; and a laterally grown portion (108a) (see Fig. 2) extending laterally from the post over the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

However, Zheleva et al. do not specifically disclose the dimension of the post size and spacing being 100 nm or less.

Brueck et al. disclose a semiconductor structure periodic pattern having dimension less than 100 nm, particularly, 30 nm using fine line interferometer lithography. As Brueck et al., disclose such small dimension devices are useful for high-speed detectors because the signal/electrical transmission across the nano regime (submicron) dimension gap determine the speed of the device (see Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Zheleva et al. reference with dimension of the post in submicron regime as taught by Brueck et al. in order to increase the speed and performance of the device.

Furthermore, the dimension outside the disclosure of Zheleva et al. and Brueck et al. can routinely optimized as the device performance and size required.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claims 2 and 3, as applied to claim 1 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein the post is formed by sub-micron lithography (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Furthermore, edge definition lithography process has no patentable weight in the product claim. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Re claim 4, as applied to claim 1 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein the laterally grown portion is spaced vertically from the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 7, as applied to claim 1 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein the laterally grown portion comprises outermost flat fronts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claims 6 and 8, as applied to claim 1 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including growing the laterally grown portion.

With regard wherein the laterally grown portion comprises outermost pointed fronts or generally triangular shape Examiner takes an Official notice because it is well-known in the art that group III-V semiconductor such GaN other are can be easily grown hexagonal or pyramidal structure having pointed face See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claims 17, 20 and 21, Zheleva et al. disclose a semiconductor structure comprising: a substrate (102) including a plurality of posts (106), each post having a predetermined size pitch size; and each post (106) having a laterally grown portion (108a) extending laterally over the substrate (see Fig. 2), wherein a spacing distance separating the laterally grown portions of the posts has predetermined length (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

However, Zheleva et al. do not specifically disclose the dimension of the post size and spacing being 100 nm or less and separating distance of the laterally growth portions.

Brueck et al. disclose a semiconductor structure periodic pattern having dimension less than 100 nm, particularly, 30 nm using fine line interferometer lithography. As Brueck et al., disclose such small dimension devices are useful for high-speed detectors because the signal/electrical transmission across the nano regime (submicron) dimension gap determine the speed of the device (see Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Zheleva et al. reference with dimension of the post in submicron regime as taught by Brueck et al. in order to increase the speed and performance of the device.

Furthermore, the dimension outside the disclosure of Zheleva et al. and Brueck et al. can routinely optimized as the device performance and size required.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner*

v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claims 18 and 19, as applied to claim 17 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein the post is formed by sub-micron lithography (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Furthermore, edge definition lithography process has no patentable weight in the product claim. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Re claims 22 and 24, as applied to claim 17 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including growing the laterally grown portion.

With regard wherein the laterally grown portion comprises outermost pointed fronts or generally triangular shape Examiner takes an Official notice because it is well-known in the art that group III-V semiconductor such GaN other are can be easily grown hexagonal or pyramidal structure having pointed face See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 23, as applied to claim 17 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein each laterally grown portion comprises

outermost flat fronts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 25, as applied to claim 17 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including a molecular electronics device attached between the laterally grown portions of the posts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 26, as applied to claim 17 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein the laterally grown portions are coalesced to form a layer (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 27, as applied to claim 19 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein the coalesced layer has reduced dislocation defects (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 28, as applied to claim 17 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein the posts comprise a plurality of three-dimensional interconnect nodes (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 29, as applied to claim 28 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including a molecular electronic device attached between at least two of the interconnect nodes (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 38, Zheleva et al. disclose a semiconductor structure comprising: a substrate (102) including a plurality of posts (106), each post having predetermined pitch; and each post having a laterally grown portion (108a) extending laterally over the substrate, wherein the laterally grown portions extend and coalesce to form a coalesced layer (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

However, Zheleva et al. do not specifically disclose the dimension of the post size and spacing (pitch side) being 100 nm or less.

Brueck et al. disclose a semiconductor structure periodic pattern having dimension less than 100 nm, particularly, 30 nm using fine line interferometer lithography. As Brueck et al., disclose such small dimension devices are useful for high-speed detectors because the signal/electrical transmission across the nano regime (submicron) dimension gap determine the speed of the device (see Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Zheleva et al. reference with dimension of the post in submicron regime as taught by Brueck et al. in order to increase the speed and performance of the device.

Furthermore, the dimension outside the disclosure of Zheleva et al. and Brueck et al. can routinely optimized as the device performance and size required.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are

otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claim 39, as applied to claim 38 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein each post is formed by sub-micron lithography (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 42 and 46, Zheleva et al. disclose a method for forming a laterally grown semiconductor structure comprising: forming at least one post on a substrate (102), the post (106) having a predetermined width; and growing a laterally grown portion (108a) from the post extending laterally from the post over the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

However, Zheleva et al. do not specifically disclose the dimension of the post size and spacing (pitch side) being 100 nm or less.

Brueck et al. disclose a semiconductor structure periodic pattern having dimension less than 100 nm, particularly, 30 nm using fine line interferometer lithography. As Brueck et al., disclose such small dimension devices are useful for high-speed detectors because the signal/electrical transmission across the nano regime (submicron) dimension gap determine the

speed of the device (see Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Zheleva et al. reference with dimension of the post in submicron regime as taught by Brueck et al. in order to increase the speed and performance of the device.

Furthermore, the dimension outside the disclosure of Zheleva et al. and Brueck et al. can routinely optimized as the device performance and size required.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claim 43, as applied to claim 42 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including growing the post by sub-micron lithography (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 44, as applied to claim 43 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

With regard growing the post by edge definition lithography. Examiner takes an Official notice because it is well-known in the art that the edge definition provides structure or pattern within the nano regime . See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 45, as applied to claim 42 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including growing the laterally grown portion to be spaced vertically from the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claims 47 and 49, as applied to claim 42 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including growing the laterally grown portion.

With regard wherein the laterally grown portion comprises outermost pointed fronts or generally triangular shape Examiner takes an Official notice because it is well-known in the art that group III-V semiconductor such GaN other are can be easily grown hexagonal or pyramidal structure having pointed face See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 48, as applied to claim 42 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including growing the laterally grown

portion structure wherein the laterally grown portion comprises outermost flat fronts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 58 and 62, Zheleva et al discloses a method for forming a laterally grown semiconductor structure comprising: forming a plurality of posts (106) on a substrate (102), each post having a predetermined width; and growing a laterally grown portion (108a) from each of the posts (106) extending laterally over the substrate (102), wherein a spacing distance separating the laterally grown portions of the posts spaced at predetermined distance (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

However, Zheleva et al. do not specifically disclose the dimension of the post size and spacing being 100 nm or less and separating distance of the laterally growth portions.

Brueck et al. disclose a semiconductor structure periodic pattern having dimension less than 100 nm, particularly, 30 nm using fine line interferometer lithography. As Brueck et al., disclose such small dimension devices are useful for high-speed detectors because the signal/electrical transmission across the nano regime (submicron) dimension gap determine the speed of the device (see Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Zheleva et al. reference with dimension of the post in submicron regime as taught by Brueck et al. in order to increase the speed and performance of the device.

Furthermore, the dimension outside the disclosure of Zheleva et al. and Brueck et al. can routinely optimized as the device performance and size required.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Re claim 59, as applied to claim 58 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including wherein each post is formed by sub-micron lithography (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 60, as applied to claim 59 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

With regard growing the post by edge definition lithography. Examiner takes an Official notice because it is well-known in the art that the edge definition provides structure or pattern

within the nano regime . See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 61, as applied as applied to claim 58 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including growing each laterally grown portion to be spaced vertically from the substrate (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claims 63 and 65, as applied to claim 58 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including growing the laterally grown portion.

With regard wherein the laterally grown portion comprises outermost pointed fronts or generally triangular shape Examiner takes an Official notice because it is well-known in the art that group III-V semiconductor such GaN other are can be easily grown hexagonal or pyramidal structure having pointed face See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942).See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 64, as applied to claim 58 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including growing each laterally grown portion structure wherein the laterally grown portion comprises outermost flat fronts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 66, as applied to claim 58 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including attaching a molecular electronic device (310) (Fig. 15) to and between adjacent laterally grown portions of adjacent posts (see

Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 67, as applied to claim 58 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including forming a plurality of three dimensional interconnect nodes for molecular device attachment from the laterally grown posts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 68, as applied to claim 58 above, Zheleva et al. and Brueck et al. in combination disclose all the claimed limitations including attaching a molecular electronic device to and between adjacent laterally grown portions of adjacent posts (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24 and Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Re claim 69, Zheleva et al. disclose a method of controlling electron affinity in a laterally overgrown semiconductor structure, comprising: providing a substrate (102) with a plurality of posts (106) included on the substrate (102), each post having laterally overgrown portions (108a) and wherein the laterally overgrown portions of adjacent posts are spaced apart a predetermined dimension; interconnecting a molecular electronic (310) device between and to the laterally overgrown portions of adjacent posts; and controlling composition of the laterally overgrown portions to control electron affinity between the laterally overgrown portions and the molecular electronics device (see Figs. 1-15 and related text in Col. 3, line 60 – Col. 10, line 24).

However, Zheleva et al. do not specifically disclose the dimension of the post size and spacing of the laterally growth portions being in nanometer scale.

Brueck et al. disclose a semiconductor structure periodic pattern having dimension less than 100 nm, particularly, 30 nm using fine line interferometer lithography. As Brueck et al., disclose such small dimension devices are useful for high-speed detectors because the signal/electrical transmission across the nano regime (submicron) dimension gap determine the speed of the device (see Brueck et al. Figs. 1A – 10C and related text Col. 4, line 14 – Col. 7, line 50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Zheleva et al. reference with dimension of the post in submicron regime as taught by Brueck et al. in order to increase the speed and performance of the device.

Furthermore, the dimension outside the disclosure of Zheleva et al. and Brueck et al. can routinely optimized as the device performance and size required.

Notwithstanding, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure Biwa et al. (US 6,858,081) also disclose similar inventive subject matter.

Correspondence

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly D. Nguyen can be reached on (571) 272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Brook Kebede/
Primary Examiner, Art Unit 2894

/BK/
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